REMARKS

Pending Claims 9-12. In the Non-Final Office Action, Examiner Shapiro rejected pending claims 9-12 on various grounds. The Applicant responds to each as subsequently recited herein, and respectfully requests reconsideration and further examination of the present application under 37 CFR § 1.112:

A. Examiner Shapiro rejected pending claims 9, 10 and 12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,384,806 to *Matsueda* et al. in view of U.S. Patent No. 5,892,493 to *Enami* et al.

The Applicant has thoroughly considered Examiner Shapiro's remarks concerning the patentability of claims 9, 10 and 12 over *Matsueda* in view of *Enami*. The Applicant has also thoroughly read *Matsueda* and *Enami*. To warrant this 35 U.S.C. §103(a) rejection of claims 9, 11 and 12, all the claim limitations recited in independent claim 9 must be taught or suggested by the combination of *Matsueda* and *Enami*. See, MPEP §2143. The Applicant respectfully traverses this §103(a) rejection of claims 9, 10 and 12, because neither *Matsueda* nor *Enami* disclose, teach or suggest "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein a first signal processing circuit associated with a first address conductor of a first group of address conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate" as recited in independent claim 9.

As to the traversal, Examiner Shapiro has correctly recognized *Matsueda*'s failure to teach or suggest the aforementioned limitation of independent claim 9. However, Examiner Shapiro has erroneously interpreted *Enami* as teaching the aforementioned limitation of independent claim 9, because a proper reading of *Enami* reveals that *Enami* also fails to teach or suggest the aforementioned limitation of independent claim 9.

Specifically, the first limitation of independent claim 9 is a substrate, which is suggested by *Enami* with the disclosure of substrates 14 and 16 as illustrated in FIG. 2.

Second, the next limitation of independent claim 9 is an array of individually addressable matrix elements carried on the substrate, which is taught by *Enami* with the disclosure of array of addressable matrix elements 18 as illustrated in FIGS. 1, 2 and 5.

Third, the next limitation of independent claim 9 is a set of address conductors connected to the array of matrix elements and carried on the substrate, which is taught by *Enami* with the disclosure of a complete set of address conductors d1A ··· dnA, d1B ··· dnB, d1C ··· dnC, and d1D ··· dnD extending from a multiplexor 38 to a LCD 10 as illustrated in FIGS. 1 and 5.

Fourth, the next limitation of independent claim 9 is the set of address conductors being arranged in a series of groups with each group including successive address conductors, which is taught by *Enami* with the disclosure of a first group A of address conductors d1A ··· dnA, a second group B of address conductors d1B ··· dnB, a third group C of address conductors d1C ··· dnC, and a fourth group D of address conductors d1D ··· dnD.

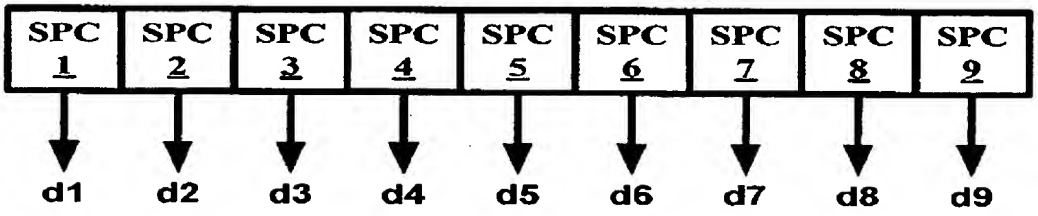
Fifth, the next two limitations of independent claim 9 are a multiplexing circuit integrated on the substrate and connected to the set of address conductors and a plurality of signal bus lines, which taught by *Enami* with the disclosure of multiplexor 38 being connected to the complete set of address conductors d1A ··· dnA, d1B ··· dnB, d1C ··· dnC, and d1D ··· dnD, and being connected to signal bus lines d1 ··· dn extending between data line driver 40 and multiplexor 38 as illustrated in FIGS. 1 and 5.

Sixth, the next limitation of independent claim 9 is the multiplexing circuit being arranged to couple sequentially each group of the set of address conductors to the plurality of signal bus lines with each address conductor in a group being coupled to a respective one of the signal bus lines. These limitations are taught *Enami* with the disclosure of (1) signal bus line d1 being coupled to address conductors d1A, d1B,

d1C and d1D; and (2) signal bus line dn being coupled to address conductors dnA, dnB, dnC and dnD as illustrated in FIGS. 1 and 5.

Seventh, the next two limitations of independent claim 9 are a plurality of signal processing circuits integrated on the substrate and each signal processing circuit being connected to a respective bus line. These limitations are taught *Enami* with the disclosure of data line driver 40 that, despite a lack of explicit description of an embodiment of data line driver 40 by *Enami*, implicitly includes a signal processing circuit for each bus line d1 ··· dn in order to process video signals from LCD controller 36 into data signals communicated by data line driver 40 to multiplexor 38 via data bus lines d1 ··· dn.

Eighth, the final limitation of independent claim 9 is each individual signal processing circuit being associated with a first address conductor of a first group and a last address conductor of a second group are adjacent on the substrate. This limitation is neither taught nor suggested by *Enami* by the disclosure of an order in which the signal processing circuits of data line driver 40 are arranged physically on the substrate in exactly the same physical order of the signal bus lines to which the signal processing circuit blocks of data line driver 40 are respectively connected as evidenced by the following illustration of data line driver 40, wherein n = 9 for nine (9) signal processing circuits SPC1-SPC9 and nine (9) signal bus lines d1-d9.



This is identical to the teachings of the prior art illustrated in FIG. 3 of the present application. Thus, *Enami* is nothing more than a cumulative reference as to teaching an order in which signal processing circuits are arranged physically on the substrate in exactly the same physical order of the signal bus lines to which the signal processing circuit blocks are respectively connected.

Withdrawal of the rejection of independent claim 9 under 35 U.S.C. §103(a) as being unpatentable over *Matsueda* in view of *Enami* is therefore respectfully requested.

Claims 10 and 12 depend from independent claim 9. Therefore, dependent claims 10 and 12 include all of the elements and limitations of independent claim 9. It is therefore respectfully submitted by the Applicant that dependent claims 10 and 12 are allowable over *Matsueda* in view of *Enami* for at least the same reason as set forth herein with respect to independent claim 9 being allowable over *Matsueda* in view of *Enami*. Withdrawal of the rejection of dependent claims 10 and 12 under 35 U.S.C. §103(a) being unpatentable over *Matsueda* in view of *Enami* is therefore respectfully requested.

B. Examiner Shapiro rejected pending claim 11 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,384,806 to *Matsueda* et al. in view of U.S. Patent No. 5,892,493 to *Enami* et al. and in further view of U.S. Patent No. 6,144,426 to *Yamazaki* et al.

Claim 11 depends from independent claim 9. Therefore, dependent claim 11 includes all of the elements and limitations of independent claim 9. It is therefore respectfully submitted by the Applicant that dependent claim 11 is allowable over *Matsueda* in view of *Enami* and in further view of *Yamazaki* for at least the same reason as set forth herein with respect to independent claim 9 being allowable over *Matsueda* in view of *Enami*. Withdrawal of the rejection of dependent claim 9 under 35 U.S.C. §103(a) being unpatentable over *Matsueda* in view of *Enami* and in further view of *Yamazaki* is therefore respectfully requested.

New Claim 13. The Applicant respectfully asserts that new independent claim 13 is allowable over the art of record due to the failure of the art of record, particularly *Matsueda, Enami* and *Yamazaki*, to teach or suggest "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein an order in which said signal processing

circuits are arranged physically on said substrate is at least partially different than a physical order of said signal bus lines to which said signal processing circuit blocks are respectively connected" as recited in independent claim 13.

SUMMARY

Examiner Shapiro's obviousness rejections have been obviated by the remarks herein supporting an allowance of pending claims 9-12 over *Matsueda* in view of *Enami*. The Applicant has supported an allowance of new claim 13 over the art of record. The Applicant respectfully submits that claims 9-13 as listed herein fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested. If any points remain in issue that may best be resolved through a personal or telephonic interview, Examiner Shapiro is respectfully requested to contact the undersigned at the telephone number listed below.

Dated: **January 30, 2004**

Respectfully submitted,
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